TMC2255

CMOS 3 x 3, 5 x 5 Image Convolver

8 x 8 Bits, 12 MHz Data Rate

Features

- 8-bit data and coefficient input precision
- Triple 3x1 matrix-vector multiplication mode
- 3x3 and 5x5 two-dimensional convolution modes
- TTL-compatible I/O with three-state output bus
- Offered in 68-contact plastic chip carrier (PLCC)
- Built-in 8-, 9-, and 12-bit arithmetic limiter
- Two's complement, unsigned, or mixed data formats

Applications

- RGB to/from YUV/YIQ color space conversion
- 3x3 or 5x5 two-dimensional FIR filtering
- Edge enhancement and general image processing
- Robotics and image recognition
- Electronic darkroom
- Desktop publishing

Description

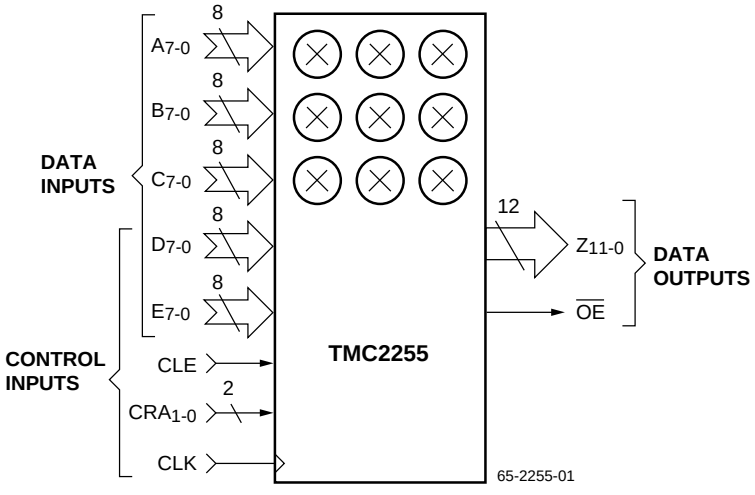
Like the faster TMC2250, the low-cost TMC2255 can perform a triple 3x1 matrix-vector multiplication or a 3x3 convolution. It can also perform a 5x5 convolution with bidimensionally symmetrical coefficients. The on-chip coefficient memory stores four sets of nine 8-bit two's complement coefficients. The device accepts unsigned and/or two's complement data at 1/3 of the applied clock rate.

The 3 (3x1) matrix multiply mode supports various 3-space numerical operations, such as video standards conversion (e.g. YIQ to RGB) or three-dimensional perspective transformation. Three input ports accept the 8-bit two's complement and/or unsigned magnitude data. The two remaining input ports can be loaded with coefficients and/or device control parameters "on-the-fly." In this mode, an output is generated on every clock cycle.

The 3x3 and 5x5 pixel image convolver modes support numerous functions, including static filtering and edge detection. On every third clock cycle, the TMC2255 accepts three (3x3 mode) or five (5x5 mode) data inputs. In the 5x5 mode, the coefficient kernel must be symmetric both horizontally and vertically. Outputs from the device are generated on every third clock cycle, matching the input pixel data rate, and can be limited ("clipped") to 8, 9, or 12 bits.

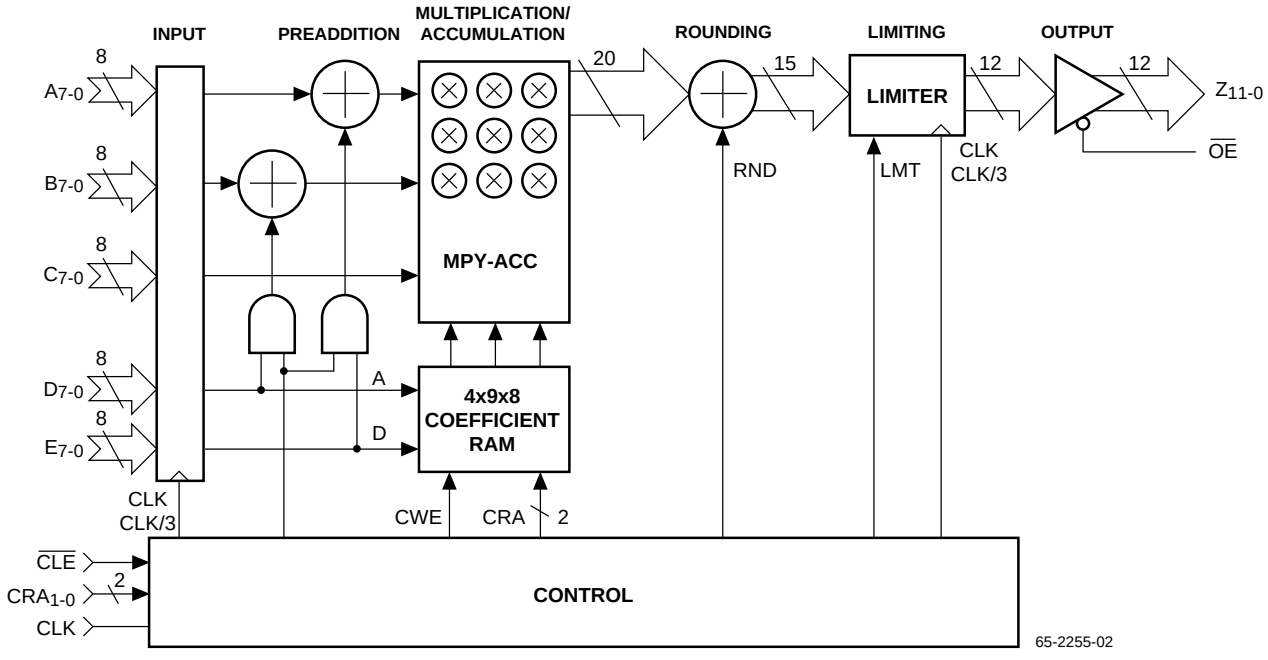
The TMC2255 will operate at clock rates of 0 to 36 MHz over the full commercial temperature (0°C to 70°C) and supply voltage ranges.

Logic Symbol



Rev. 1.0.1

Structural Block Diagram



Functional Description

The TMC2255 contains an array of multipliers and adders, four 9x8-bit coefficient "pages" and a global control block, all of which can be initialized or reconfigured through ports D and E when $\overline{CLE}$ is LOW. Device parameters include matrix coefficient, internal device configuration (mode), rounding precision, and input/output data formats (two's complement, unsigned, or mixed). After the control parameters have been loaded, device operation commences with the next clock rising edge on which $\overline{CLE}$ returns HIGH. Depending on the mode selected, three or five data are input in parallel and proceed through a sequence of operations: Input, Preaddition, Multiply-Accumulation, Rounding, Limiting, and Output. See Figures 1–3 and the Structural Block Diagram.

Input Stage

Inputs are supplied to ports A through C in all operating modes on every third clock cycle, beginning with the clock rising edge that contains the most recent $\overline{CLE}$ LOW-to-HIGH transition. Control and/or coefficient parameters can be input through ports D and E during any of the three master clock cycles that make up each data cycle. In the 5x5 convolution mode, data enter the device through ports A–E. Control and/or coefficients may be updated through ports D and E on the remaining two cycles of each clock triplet.

Input data formats may be unsigned and/or two's complement, as identified in the mode select field of port E.

Preaddition

In and only in 5x5 convolution, the horizontal and vertical symmetry of the coefficient permits nine multipliers to do the work of 25. To facilitate this, the data input into ports A and E are pre-added before multiplication, as are the B and D inputs. See Figure 3, the 5x5 Block Diagram.

Coefficient Memory

The TMC2255 contains enough memory to store four "pages" of nine 8-bit two's complement coefficients each.

When $\overline{CLE}$ is LOW, a new coefficient is written through port E to the page and location address identified on port D. On every third clock cycle, the coefficient page to be read and used in the immediate 3-cycle computation set is selected by CRA_0 and CRA_1. Of the nine coefficients per page, K1,i (i = 1 to 3) process the port A (and E) data; K2,i, the port B and (D) data; and K3,i, the port C data.

Multiplication and Accumulation

The device computes nine products during every three clock cycles, accumulating them internally to full precision.

Rounding

Accumulated sums of products are rounded before the last 5 or 6 bits are truncated. Rounding is performed by adding "010000" or "100000" to the emerging data stream, according to the desired precision of the output results. When $\overline{CLE}$ = 0 and D = 0XXX1111, pin E_6 sets the chip's rounding position, viz: E_6 = 0: add .010000 and use Z_0 as least significant bit; E_6 = 1: add .100000 and use Z_1 as least significant bit, ignoring Z_0.

Output Limiting

The device provides programmable output limiting in unsigned (UN) and/or two's complement (TC) format and for 8, 9, or 12 bits of output precision (including Z_0). In 3 (3x1) mode, for an RGB-to-YIQ transformation, the device can limit Z_1 (Y) to 9 bits unsigned while limiting Z_3 (I) and Z_3 (Q) to 9 bits two's complement.

Outputs

Output is through the 12-bit Z port, which provides 1/2 or 1 LSB precision, relative to the input format. In the 3 (3x1) mode, three outputs will appear consecutively at the Z port during each triple clock cycle; for data input on clock rising edge 0, these results will emerge t_{DO} after clock rising edges 7, 8, and 9. In both convolution modes the results are output at 1/3 the device master clock rate, with the first point of the impulse response emerging after clock rising edge 9. To facilitate connection to a bus, the output buffers are enabled and disabled (placed in high-impedance state) by asynchronous control $\overline{OE}$.

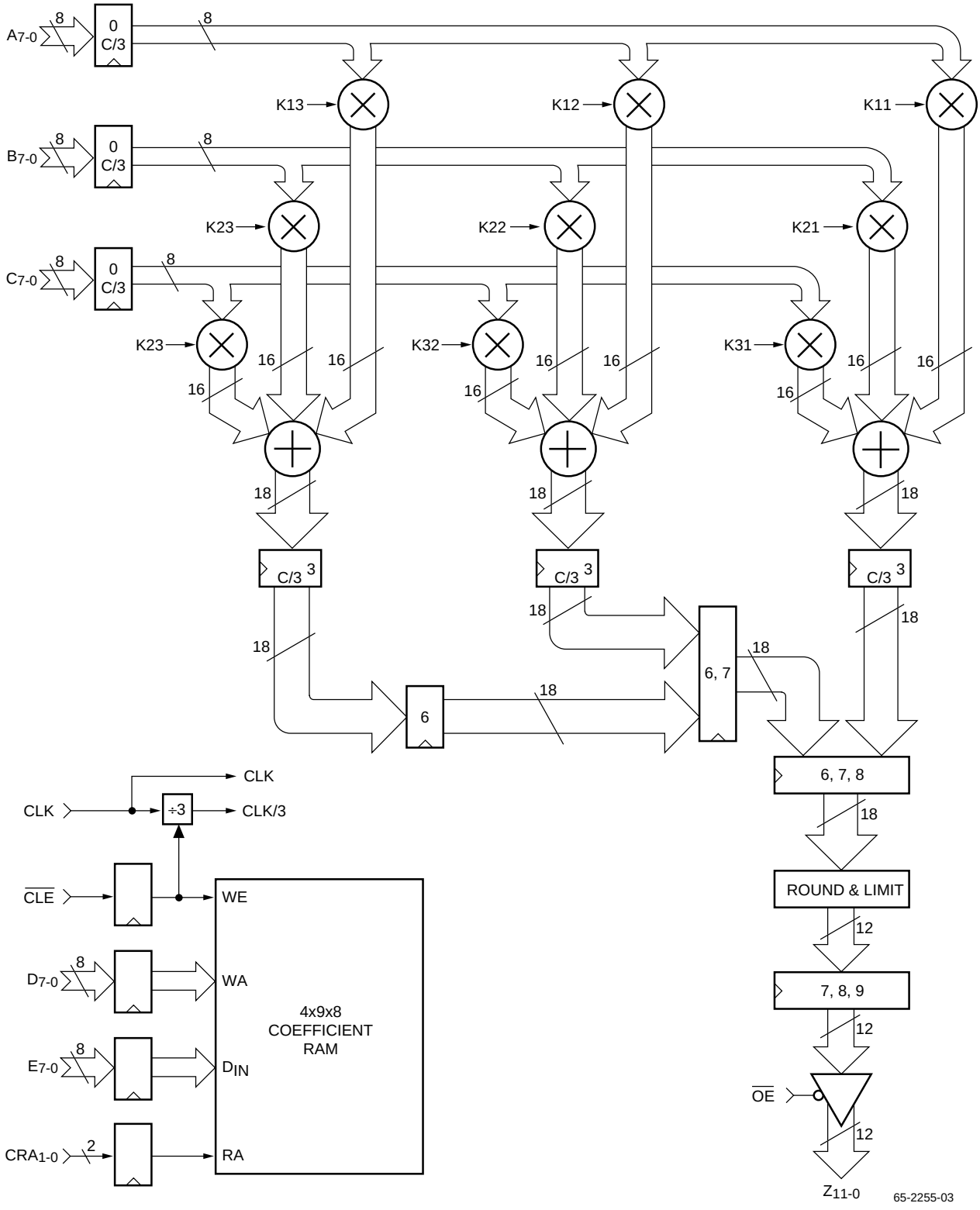


Figure 1. Functional Block Diagram, 3 (3x1) Mode

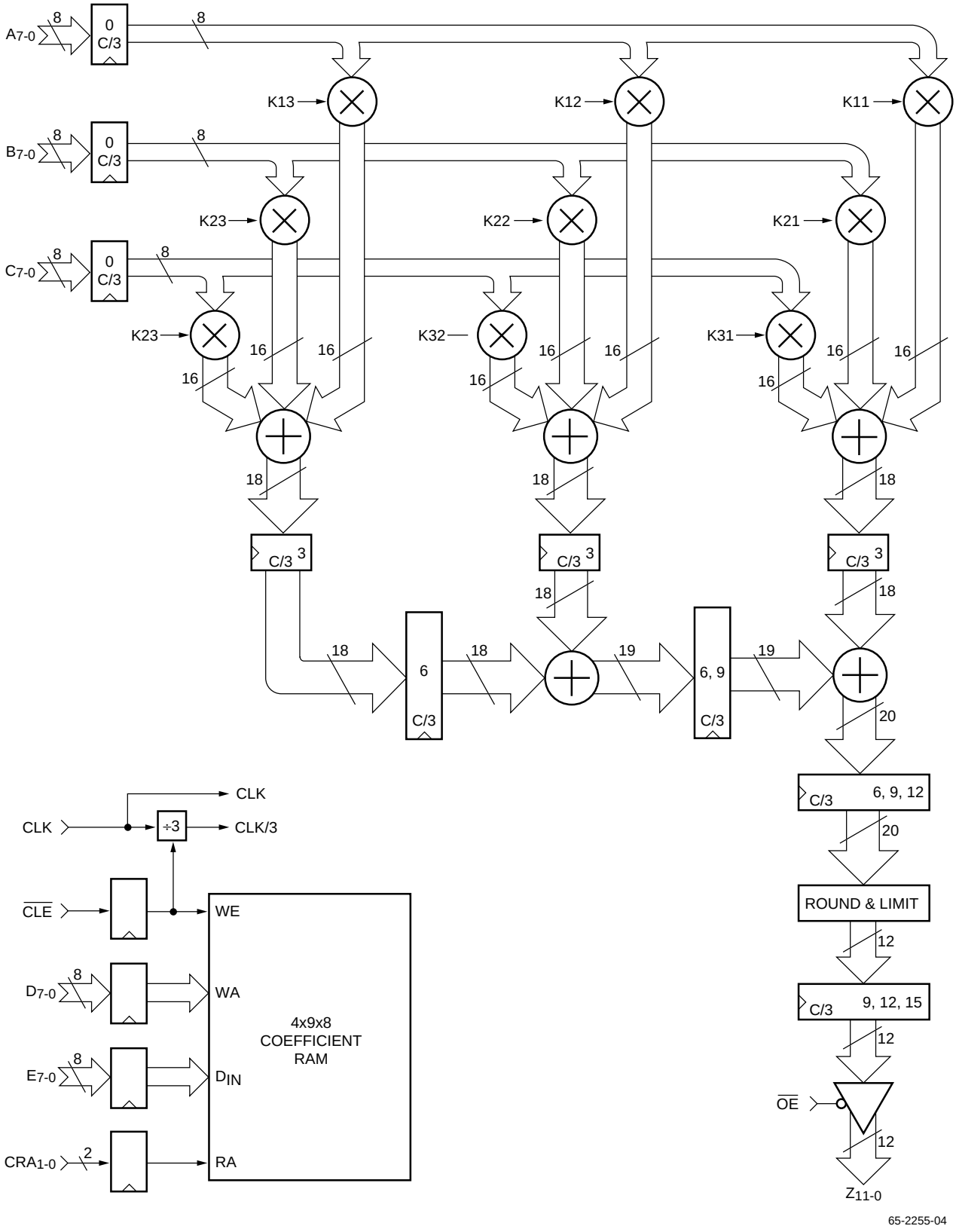


Figure 2. Functional Block Diagram, 3x3 Mode

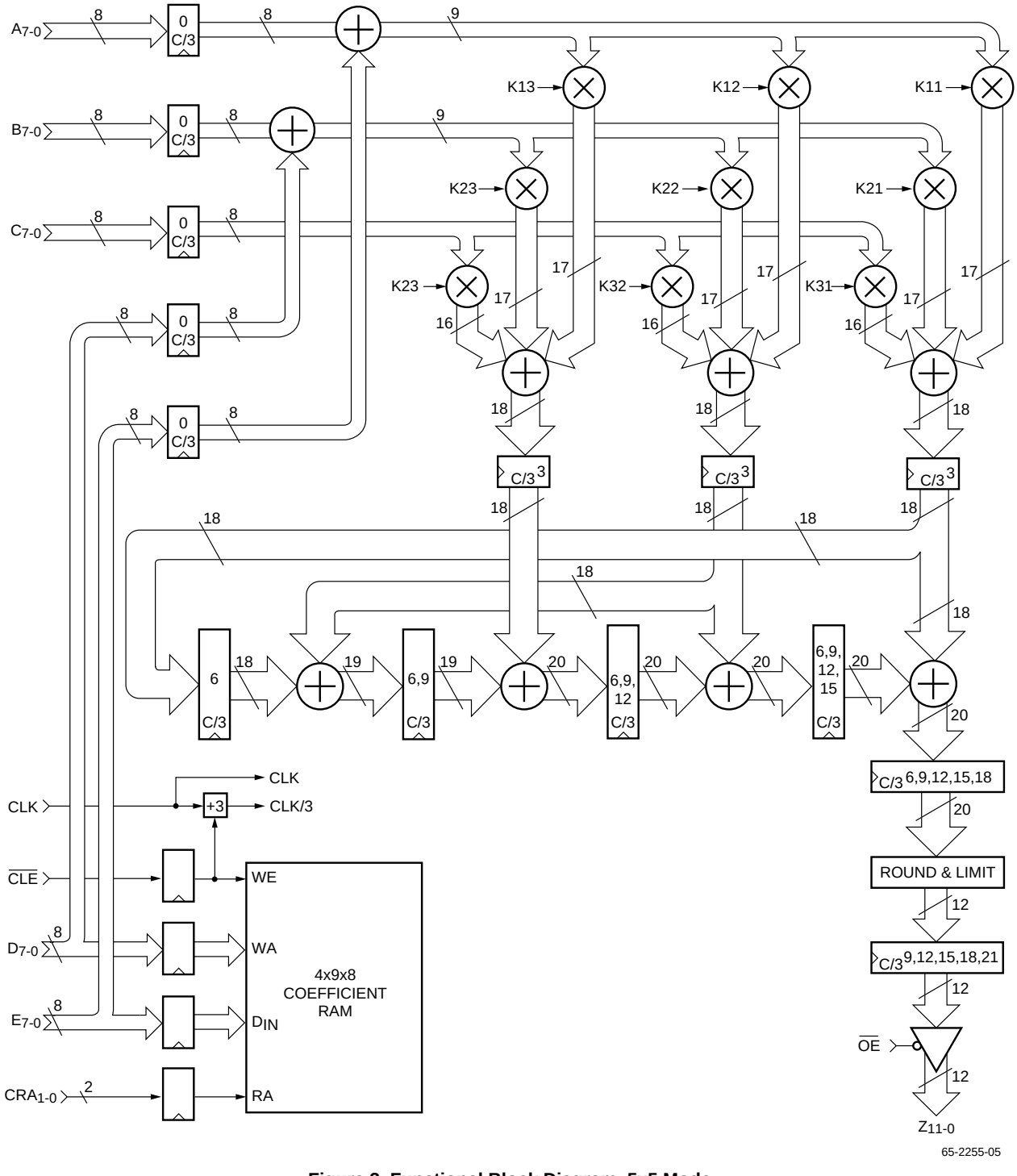
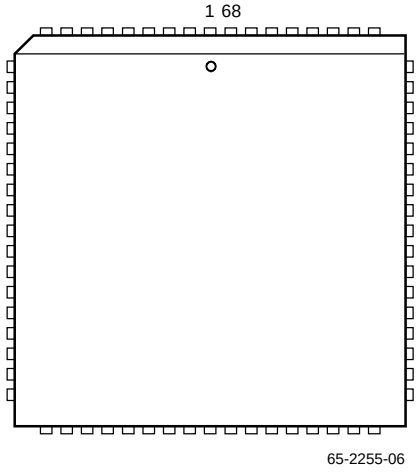


Figure 3. Functional Block Diagram, 5x5 Mode

Pin Assignments



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	18	GND	35	GND	52	GND
2	V_{DD}	19	Z_6	36	D_7	53	V_{DD}
3	A_2	20	Z_5	37	D_6	54	B_7
4	A_1	21	Z_4	38	D_5	55	B_6
5	A_0	22	Z_3	39	D_4	56	B_5
6	$\overline{CLE}$	23	Z_2	40	D_3	57	B_4
7	$\overline{OE}$	24	Z_1	41	D_2	58	B_3
8	CLK	25	Z_0	42	D_1	59	B_2
9	GND	26	GND	43	D_0	60	B_1
10	V_{DD}	27	E_7	44	C_7	61	B_0
11	Z_{11}	28	E_6	45	C_6	62	CRA_1
12	Z_{10}	29	E_5	46	C_5	63	CRA_0
13	GND	30	E_4	47	C_4	64	A_7
14	Z_9	31	E_3	48	C_3	65	A_6
15	Z_8	32	E_2	49	C_2	66	A_5
16	Z_7	33	E_1	50	C_1	67	A_4
17	V_{DD}	34	E_0	51	C_0	68	A_3

Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Inputs		
CLK	8	**Master chip clock, 0 to 30MHz.** All operations are referenced to the rising edges of CLK.
A_{0-7}, B_{0-7}, C_{0-7}, D_{0-7}, E_{0-7}	5-3, 68-64; 61-54; 51-44; 43-36; 34-27	**Data inputs.** Of the device's five 8-bit data input ports, A, B, and C are used exclusively as data inputs, whereas D and E are also used to program the device (see description of $\overline{CLE}$ pin). For 5x5 convolution, all five ports accept incoming data. In the other modes, only ports A-C accept incoming data, leaving D and E dedicated to control and coefficient values, which may be updated at any time. In all modes, data are loaded on every third rising edge for which $\overline{CLE}$ makes a 0-to-1 transition. Bits A_7, B_7,… are the two's complement sign bits or most significant unsigned bitsl bits A_0, B_0,… are the least significant bits (LSBs).
$\overline{CLE}$	6	**Active-LOW coefficient and control load enable.** When $\overline{CLE}$ is LOW, E becomes the input port for the coefficients, and D becomes the coefficient write address and control port. When $\overline{CLE}$ is HIGH, all coefficients are held unchanged. A LOW-to-HIGH transition at $\overline{CLE}$ also synchronizes the TMC2255, ushering in a new data input.
CRA_{1-0}	62-63	**Coefficient read address.** The chip can hold four "pages" of nine coefficients each. These two pins determine which of the four coefficient sets is to be used with the data entering during that cycle. The timing of coefficient selection by CRA is mode dependent. In the 3 (3x1) mode, CRA influences all coefficients simultaneously. In the 3x3 and 5x5 convolution modes, however, CRA selects the coefficients for each multiplier column individually, i.e. three per clock cycle from left to right (see Figure 3). CRA should be changed only on "data input" clock cycles to avoid corrupting 3x3 or 3 (3x1) work in progress. CRA should not be updated during a 5x5 operation whose result is needed. When updating coefficients on-the-fly, the user should not set CRA_{1-0} and D_{5-4} to the same page, but should read from one page while writing to another.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
$\overline{OE}$	7	**Asynchronous, active-LOW output enable.** When $\overline{OE}$ is LOW, the output drivers are enabled. When $\overline{OE}$ is HIGH, they are disabled (high-impedance).
Outputs		
Z_{11-0}	25-19, 16-14, 12-11	**Data outputs.** Outputs available on the Z port are enabled by $\overline{OE}$. Z_{11} is the unsigned MSB or two's complement MSB/sign bit; Z_1 is the integer LSB ("ones' digit"). Z_0 is the 1/2 fractional digit. In the 3 (3x1) mode (E = XXXXX0XX), a new valid result will emerge t_{DO} after every rising edge of CLK. In the other modes (E = XXXXX1XX), a result emerges after every third rising edge of CLK. Then 9-bit limiting is used, bits Z_{11} through Z_8 will be identical.
Power		
GND	1, 9, 13, 26, 35, 52	Ground.
VDD	2, 10, 17, 53	Supply Voltage (+5).

Operation and Timing

Before operation, the TMC2255 must be initalized, i.e. loaded with coefficients and set to the desired operating mode, data format, and rounding precision. The chip is programmed via ports D and E, which double as data input ports in 5x5 mode.

Initialization

Chip Select

This control is accessed through bit 7 of port D. When $\overline{CLE}$ is LOW, D_7 must be LOW to allow the coefficient/control information to be updated. If D_7 is HIGH when $\overline{CLE}$ is force LOW, the device will not allow the coefficient or control information to be updated, and device execution will begin or continue as commanded on the previous LOW-to-HIGH transition of $\overline{CLE}$. Holding D_7 HIGH (at least when $\overline{CLE}$ is LOW) permits the system to resynchronize the chip without changing any coefficients or configuration parameters.

Coefficient Loading

When $\overline{CLE}$ and D_7 are LOW, the coefficient values presented to port 6 are loaded into the coefficient position and page registers selected by port D, as shown in Table 1.

Each of the four “pages” YY comprises a full set of nine coefficients (one per filter tap).

Table 1. Coefficient Loading

When D_{7-0} =	Update from E_{7-0}: Coef	Page
0XYY0000	1,1	YY
0XYY0001	1,2	YY
0XYY0010	1,3	YY
0XYY0100	2,1	YY
0XYY0101	2,2	YY
0XYY0110	2,3	YY
0XYY1000	3,1	YY
0XYY1001	3,2	YY
0XYY1010	3,3	YY
0XXX0X11	Hold all coefficients	
0XXX011	Hold all coefficients	
0XXX110X	Hold all coefficients	
0XXX11X0	Hold all coefficients	
0XXX1111	Control information	
1XXXXXXX	Hold all coefficients	

X = Don’t Care

Mode Selection

When $\overline{CLE}$ = 0 and D = 0XXX1111, pins E_{2-0} select the chip’s operating MODE and input data formats, as shown in Table 2.

Table 2. Mode Selection

When E_{7-0} =	Mode =	Data Formats		
		A	B	C
0XXXX000	3 (3x1) mat mpy	TC	TC	TC
0XXXX001	3 (3x1) mat mpy	UN	TC	TC
0XXXX010	RESERVED—Do not use			
0XXXX011	3 (3x1) mat mpy	UN	UN	UN
Z1 = A*K1,1 + B*K2,1 + C*K3,1		First of 3 results		
Z2 = A*K1,2 + B*K2,2 + C*K3,2				
Z3 = A*K1,3 + B*K2,3 + C*K3,3		Last of 3 results		
0XXXX100	3x3 convolution	TC	TC	TC
0XXXX101	3x3 convolution	UN	UN	UN
Z = A1*K1,1 + B1*K2,1 + C1*K3,1 + A2*K1,2 + B2*K2,2 + C2*K3,2 + A3*K1,3 + B3*K2,3 + C3*K3,3				
0XXXX110	5x5 convolution	TC	TC	TC
0XXXX111	5x5 convolution	UN	UN	UN
Z = A1*K1,3 + B1*K2,3 + C1*K3,3 + D1*K2,3 + E1*K1,3 + A2*K1,2 + B2*K2,2 + C2*K3,2 + D2*K2,2 + E2*K1,2 + A3*K1,1 + B3*K2,1 + C3*K3,1 + D3*K2,1 + E3*K1,1 + A4*K1,2 + B4*K2,2 + C4*K3,2 + D4*K2,2 + E4*K1,2 + A5*K1,3 + B5*K2,3 + C5*K3,3 + D5*K2,3 + E5*K1,3				
1XXXXXXX	Unchanged from previous setting			

Coefficients are always 8-bit two's complement.

Rounding

All computations are rounded internally following the final accumulation of products. Rounding position depends on the output format. If the user desires outputs with 1/2 LSB precision (relative to the inputs) then rounding is performed into Z_{-1}, just to the right of the LSB of the output port, Z_0. For 1 LSB precision, rounding is into Z_0, and the output is on pins Z_{11-1} only.

Table 3. Rounding

When E_{7-0} =	Outputs are	Rounded at
00XXXXXX	Z_{11}–Z_0 (12 bits)	Z_{-1}
01XXXXXX	Z_{11}–Z_1 (11 bits)	Z_{-0}
1XXXXXXX	Unchanged from previous setting	

Output Limiting

When $\overline{CLE}$ = 0 and D = 0XXX1111, pins E_{5-3} tell the chip to which numerical format(s) to limit the emerging results. Unsigned (UN), two's complement (TC), and mixed data formats of 8, 9, or 12 bits (including Z_0) are supported, as shown in Table 4. Limit "Z" applies to 3x3 and 5x5 convolutional modes; limits Z1, Z2, Z3 apply to 3(3x1) mode.

Prior to output, the limiter (if enabled) tests the leading bits of the emerging result. In the unsigned limit modes, if the MSB = 1, denoting a negative value, the output is forced to 0; if the MSB = 0 but any other bit above the 8, 9, or 12 bit output field = 1, the output is forced to 11111111111.1. In the TC9 limit mode, values above 127.5 (00001111111.1) are forced to 00001111111.1 and values below -128 become 11110000000.0. In the TC12 limit mode, values above 1023.5 (01111111111.1) are forced to 01111111111.1, and values below -1024 become 10000000000.0. If full LSB rounding (E_6 = 1) is used, output bit Z_0 is ignored, each data format is correspondingly 1 bit narrower than shown in Table 4, and the .5 fractions disappear from the range limits.

Table 4. Output Limiting

E_{7-0} =	Limit Z1 or Z	Limit Z2	Limit Z3	Range (RND = 0)
0X000XXX	Limiter disabled			
0X001XXX	UN9	UN9	UN9	0, 255.5
0X010XXX	TC12	TC12	TC12	-1024, 1023.5
0X011XXX	UN12	UN12	UN12	0, 2047.5
0X100XXX	TC9	TC9	TC9	-128, 127.5
0X101XXX	UN9	TC9	TC9	(Mixed)
0X110XXX	Reserved—Do not use			
0X111XXX	UN8	UN8	UN8	0, 127.5
1XXXXXXX	Unchanged from previous setting			

Timing

Result Latency

Device operating mode affects when valid results are available at the output port Z_{11-0}. The three results of a 3x1 triple dot product whose inputs enter on clock rising edge 0 will be available t_{DO} after clock rising edges 7, 8, and 9. In a 3x3 and 5x5 convolution, the first three impulse response points will emerge after clock rising edges 9, 12, and 15. The last two points of a 5-point response (5x5 mode) will follow after rising edges 18 and 21.

Instructions, Inputs, and Synchronization

Each rising edge of CLK which bears a $\overline{CLE}$ LOW-to-HIGH transition resynchronizes the device. If $\overline{CLE}$ goes from LOW to HIGH on clock rising edge N, then the chip will resynchronize, starting a new 3-cycle sequence on that edge. It will look for incoming data at clock rising edges N+3i, where i = 1, 2, … (see Figures 4 through 10). If $\overline{CLE}$ is brought LOW while an operation is already in progress (e.g., to update coefficients), it should be brought HIGH only on a regular data input clock cycle (N+3i), to avoid corrupting pending results.

IF $\overline{CLE}$ is LOW, control and/or coefficient information enetering on a rising edge of CLK will affect all subsequent data inputs until the control parameters are again updated. Internal pipelining of the controls ensures that “in progress” operations on data previously input into the device will continue unaffected, as long as $\overline{CLE}$ is brought HIGH only on data input clock edges.

System Timing

Because the TMC2255’s data throughput rate is 1/3 of its incoming clock rate, the user must synchronize the data inputs with the chip’s control inputs and internal operation. Figures 4 through 7 illustrate four ways to use rising edges of $\overline{CLE}$ to align data inputs in the 3 (3x1) and 3x3 modes, whereas Figures 8 through 10 show how to use $\overline{CLE}$ in the 5x5 mode.

In Figure 4, the $\overline{CLE}$ 0-to-1 transition on CLK rising edge 3 (t = 3) initialized the chip. The final configuration and coefficient values are loaded through ports D and E at t = 2 and the first incoming data enter ports A, B, and C on rising edge 6. In 3 (3x1) mode, the three results from the t = 6 input data emerge after t = 13, 14, and 15. In 3x3 mode, the first result from the edge 6 input data appears after edge 15 and remains until t = 18, when the second result using t = 6 inputs (which is the first result using t = 9 inputs) emerges. After t = 18, the convolution of the t = 6, t = 9, and t = 12 inputs, the last output involving the t = 6 input, appears. The part operates continuously, with inputs read on every third rising clock edge and a new output available t_{DO} after each rising clock edge (3 (3x1) mode) or every third rising edge (3x3 mode).

In Figure 5, CLK rising edges at t = 3, 6, 9, … resynchronize the chip, with configuration or coefficient updates at t = 2, 5, 8, … . Data input/output timing is unchanged from Figure 3.

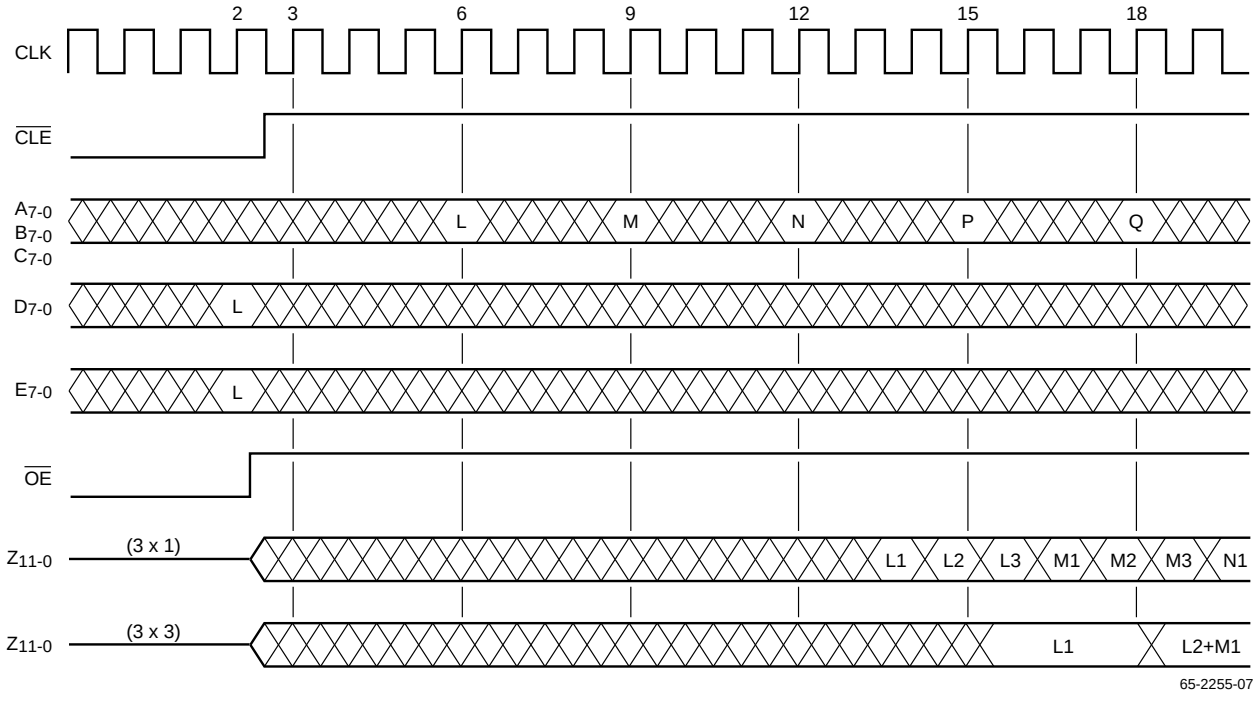


Figure 4. 3 (3x1), 3x3 Timing Diagram, Single $\overline{\text{CLE}}$ Rising Edge

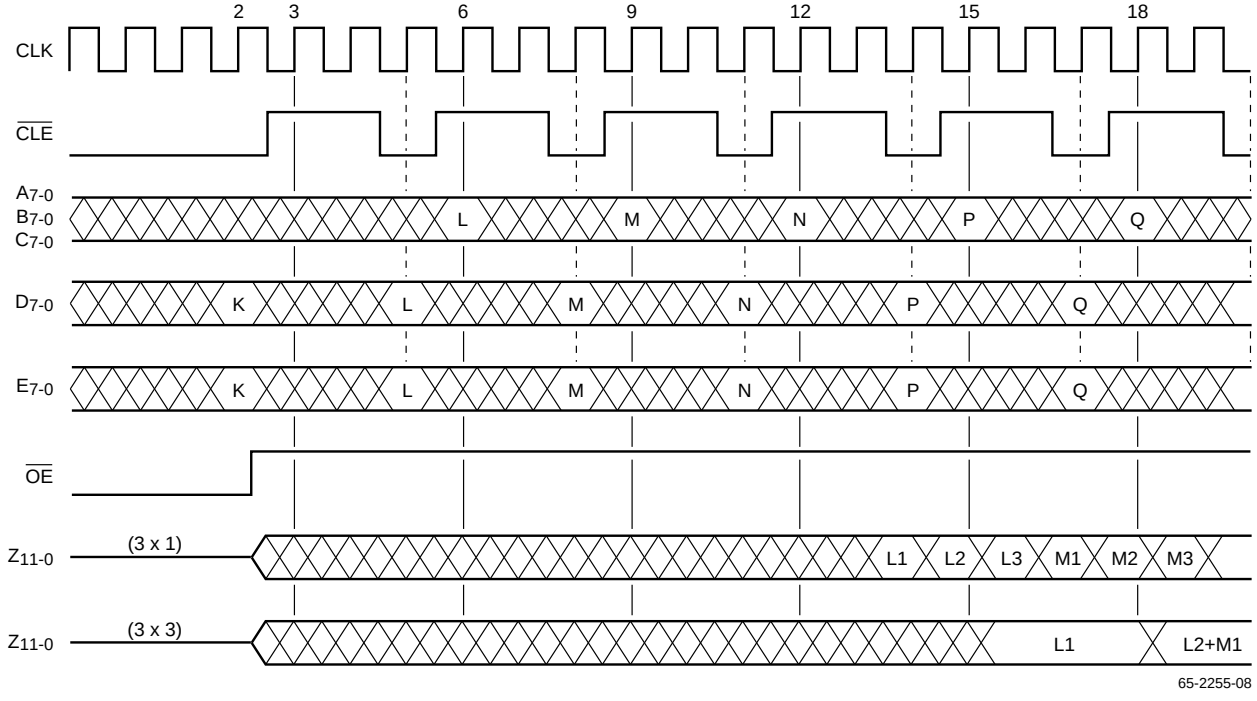


Figure 5. 3xX Modes, Periodic Long $\overline{\text{CLE}}$ Pulses

In Figure 6, CLK rising edges at t = 3, 6, 9, … again resynchronize the chip, but configuration and coefficients my be changed twice as often, at t = 1, 2, 4, 5, 7, 8, … .

In Figure 7, data timing is the sames as that of Figure 4. However, since $\overline{CLE}$ is left LOW after the one-cycle initialization pulse, instructions and coefficients may be updates on every clock cycle, or three times per data input. Instructions entering between data values, e.g. at t = 4 or t = 5, affect the next data value (i.e., that entering at t = 6). Instructions entering with a given data value (e.g., t = 6) affect the next data input (i.e., at t = 9).

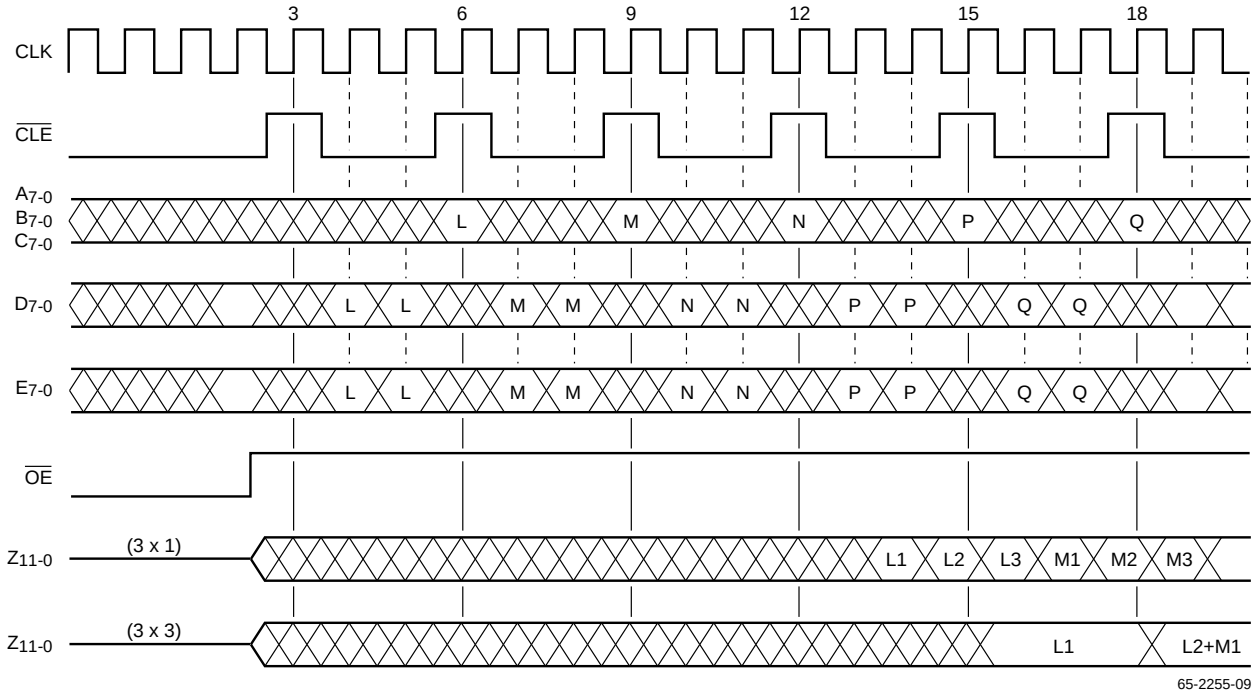


Figure 6. 3xX Modes, Periodic Short $\overline{CLE}$ Pulses

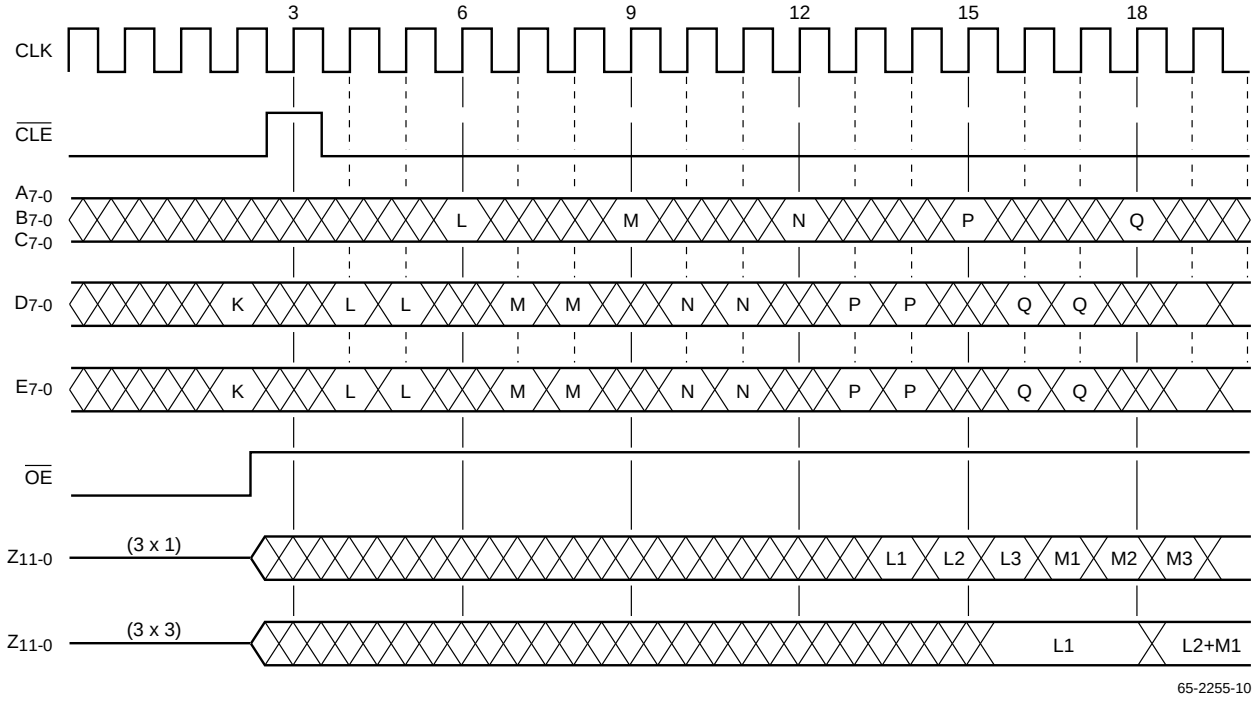


Figure 7. 3xX Modes, Single $\overline{CLE}$ Rising Edge

In Figure 8, the CLK rising edge at t = 3 synchronizes the operation. The final configuration and coefficient values are loaded through ports D and E at t = 2, and the first incoming data enter ports A through E at t = 6. The first results using the t = 6 input appears after t = 15 and remains until t = 18. The last result using the t = 6 input emerge after t = 27 and remains until t = 30. The part operates continuously, with data inputs read on every third rising edge of CLK and a new output available t_{DO} after every third rising edge of CLK.

In Figure 9, one new coefficient or configuration value can be input for every data input, at t = 5, 8, 11, … .

In Figure 10, two new coefficients or configuration values can be loaded for every incoming data point, at t = 4, 5, 7, 8, 10, 11, … .

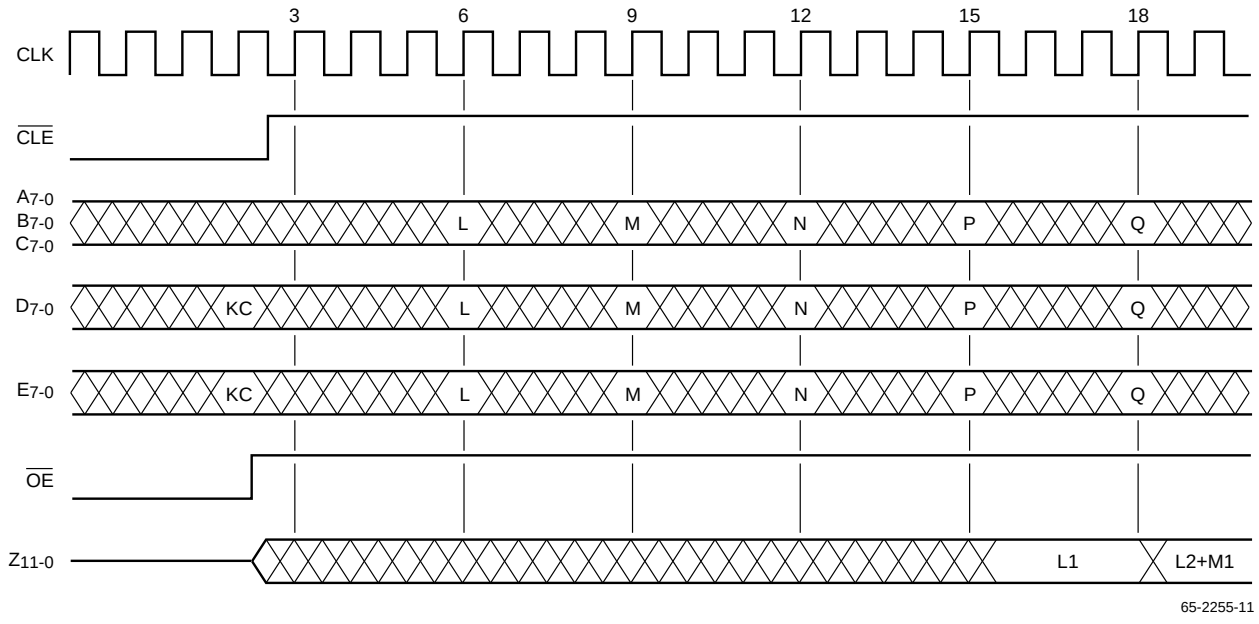


Figure 8. 5x5 Convolution, Single $\overline{CLE}$ Rising Edge

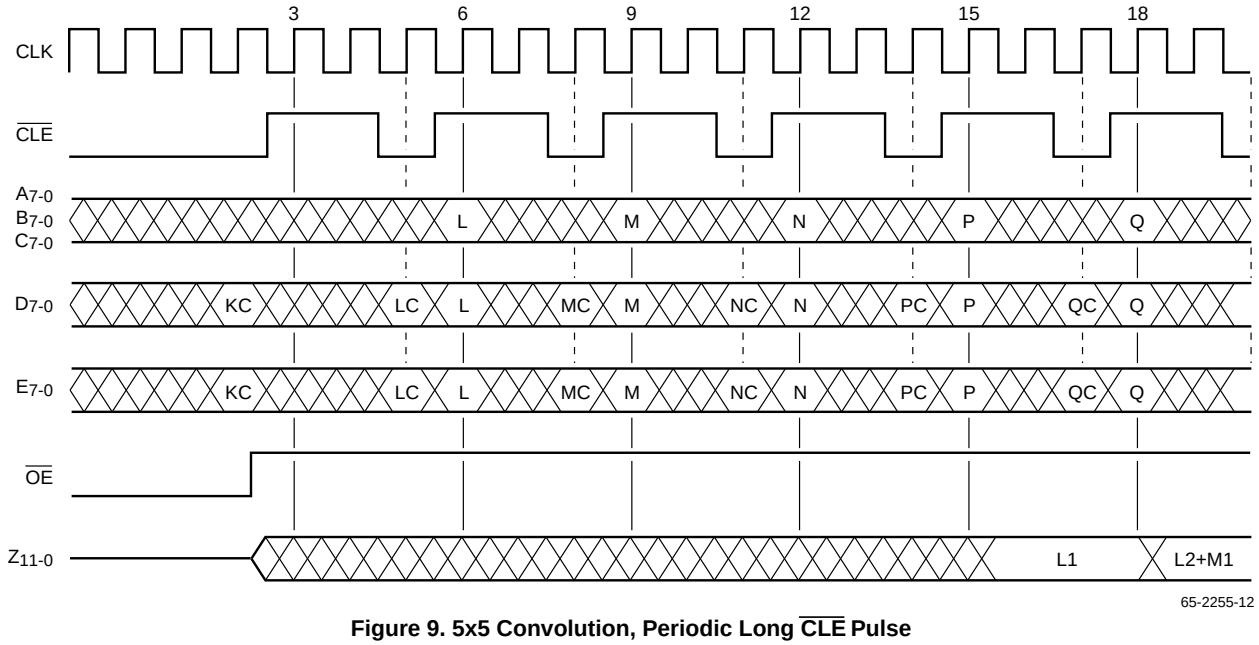


Figure 9. 5x5 Convolution, Periodic Long $\overline{CLE}$ Pulse

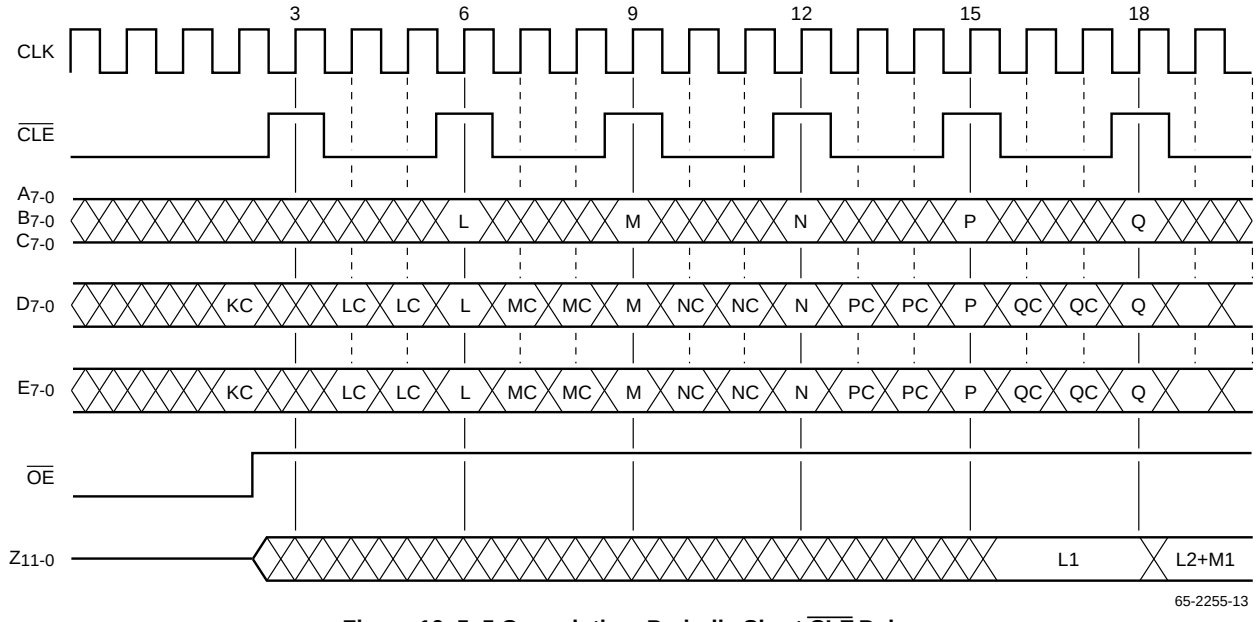


Figure 10. 5x5 Convolution, Periodic Short $\overline{\text{CLE}}$ Pulse

In 5x5 mode, $\overline{\text{CLE}}$ should not be left LOW continuously, since ports D and E must serve as data inputs on every third clock cycle. If $\overline{\text{CLE}}$ is LOW on a data input cycle, the chip will interpret the current D and E inputs as both data and instructions/coefficients.

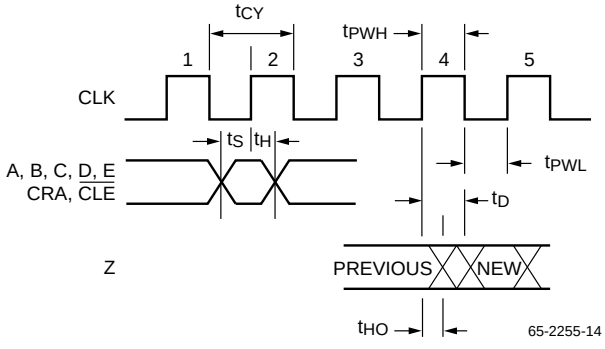


Figure 11. I/O Timing Diagram

Power-Up Sequence

To ensure proper operation, the TMC2255 should receive at least two clock rising edges soon after power-up, with $\overline{\text{CLE}}$ making a 0-to-1 transition on edge 4, 5, or 6. Otherwise, some of the internal multiplexers will power up in disallowed states and draw excessive power.

Data Formats

Figure 12 summarizes the TMC2255's data and coefficient formats for all operating modes. Although integer weighting of input data is shown, the binary point may be moved anywhere to the left, as long as the binary point of the output is moved the same distance. Likewise, the coefficient binary point can be moved, as long as the output binary point is moved equally or the data input binary point is moved in the opposite direction. In all coefficients and in all two's complement data, the most significant bit carries a negative weighting.

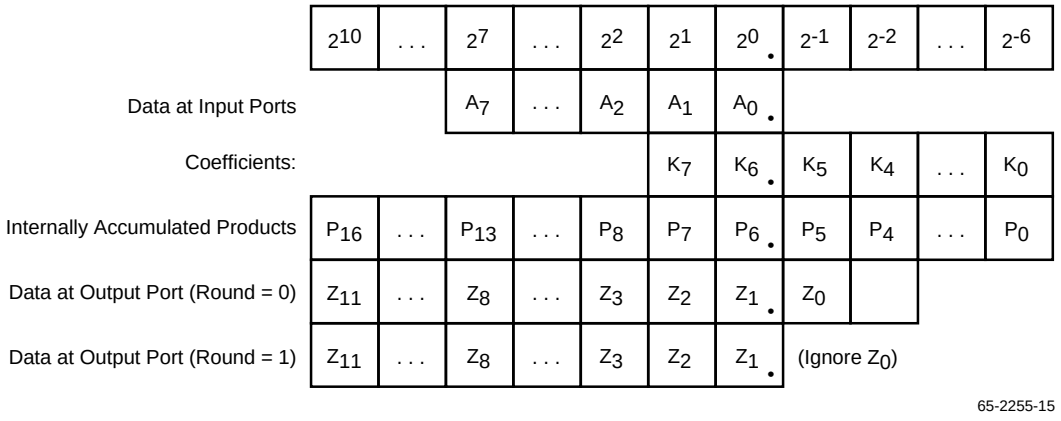


Figure 12. Data Formats and Bit Alignment

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Output Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Output Forced Current[3,4]	-6.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating Case Temperature	-60		130	°C
Junction Temperature			175	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Package	Min	Nom	Max	Unit
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
V_{IL}	Input Voltage LOW				0.8	V
V_{IH}	Input Voltage HIGH		2.0			V
I_{OL}	Output Current LOW				4.0	mA
I_{OH}	Output Current HIGH				-2.0	mA
t_{CY}	Cycle Time	TMC2255	33			ns
		TMC2255-1	27			
t_{PWL}	Clock Pulse Width LOW	TMC2255	16			ns
		TMC2255-1	14			
t_{PWH}	Clock Pulse Width HIGH	TMC2255	13			ns
		TMC2255-1	10			
t_S	Input Setup Time	TMC2255	8			ns
		TMC2255-1	6			
t_H	Input Hold Time		0			ns
t_A	Ambient Temperature		0	25	70	°C

Electrical Characteristics

Parameter		Test Conditions	Min	Max	Unit
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max., V_{IN} = 0		15	mA
I_{DDU}	Supply Current, No Load	V_{DD} = Max., t_{CY} = 50ns		100	mA
I_{IL}	Input Current LOW			-10	µA
I_{IH}	Input Current, HIGH			10	µA
V_{OL}	Output Voltage, LOW			0.4	V
V_{OH}	Output Voltage, HIGH		2.0		V
I_{OS}	Short-Circuit Output Current			-100	µA
C_I	Input Capacitance			10	pF
C_O	Output Capacitance			10	pF

Note: Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching Characteristics

Parameter		Test Conditions	Package	Min	Max	Unit
t_D	Output Delay	V_{DD} = Min., C_L = 25pF	TMC2255		22	ns
			TMC2255-1		19	
t_{HO}	Output Hold	V_{DD} = Max., C_L = 25pF			6	ns
t_{ENA}	Output Enable	V_{DD} = Min., C_L = 25pF	TMC2255		18	ns
			TMC2255-1		15	
t_{DIS}	Output Disable	V_{DD} = Min., C_L = 25pF	TMC2255		21	ns
			TMC2255-1		20	

Equivalent Circuits and Transition Levels

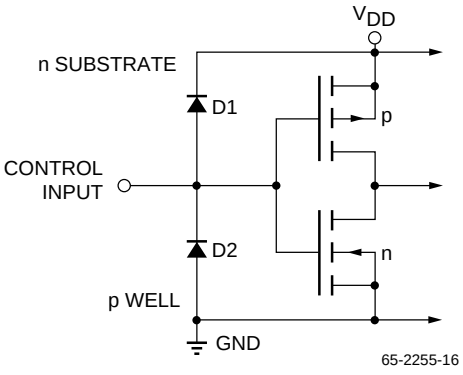


Figure 13. Equivalent Input Circuit

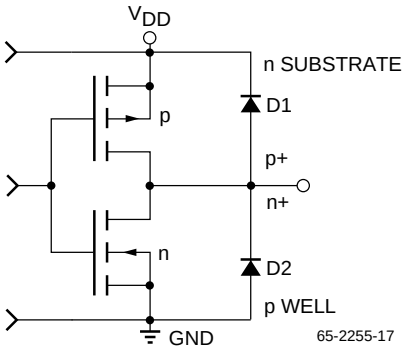


Figure 14. Equivalent Output Circuit

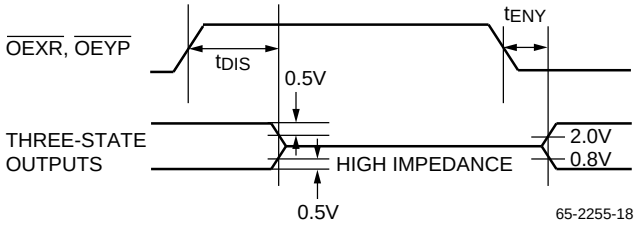


Figure 15. Transition Levels for Three-State Measurements

Related Products

- TMC2011 Variable Length Shift Resistor
- TMC2302 Image Manipulation Sequencer

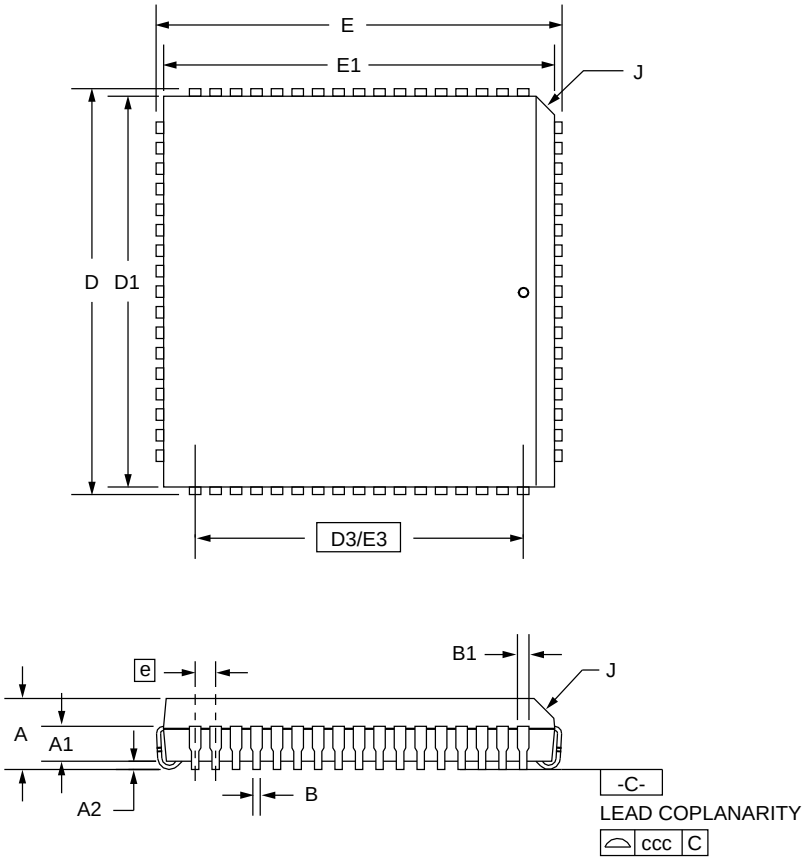
Notes:

Mechanical Dimensions – 68-Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.200	4.19	5.08	
A1	.090	.130	2.29	3.30	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.985	.995	25.02	25.27	
D1/E1	.950	.958	24.13	24.33	3
D3/E3	.800 BSC		20.32 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	17		17		
N	68		68		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Data Rate (MHz)	Temperature Range	Screening	Package	Package Marking
TMC2255R1C	10	0°C to 70°C	Commercial	68 Pin PLCC	2255R1C
TMC2255R1C1	12.5	0°C to 70°C	Commercial	68 Pin PLCC	2255R1C1

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